each sealing ring encloses at least one pump-out port of the plurality of pump-out ports; and

the first and second silicon wafers are effectively a bonded together set of wafers.

2. The method of claim 1, further comprising:

placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via the at least one pump-out port; and

depositing a layer of material on the second side of the first silicon wafer and the plurality of pump-out ports on the second side of the first silicon wafer, wherein each chamber is sealed from the environment.

3. The method of claim 2, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer and the plurality of pump-out ports on the second side of the first silicon wafer.

4. The method of claim 3, further comprising coating the second wafer with antireflection material.

5. The method of claim 4, wherein the second silicon wafer is made from low oxygen silicon or float zone silicon to minimize an absorption peak in an 8–14 micron wavelength region of light going through the second silicon wafer to the plurality of devices.

6. The method of claim 5, wherein the set of wafers is cut into a plurality of chips wherein each chip has one or more sealed chambers.

7. The method of claim 6, wherein the plurality of devices comprise thermoelectric detectors.

8. The method of claim 6, wherein the plurality of devices comprise bolometers.

9. A method for making a wafer-pair having at least one deposited layer plugged sealed chamber, comprising:

growing a first thermal layer on a first side of a first silicon wafer;

depositing a nitride layer on the first thermal layer;

depositing and patterning a first metal layer on the nitride layer for at least one device;

depositing and patterning a second metal layer on the nitride layer and the first metal layer for the at least one device;

patterning and removing material from the first silicon wafer and layers on the first side of the first silicon wafer and from a second side of the first silicon wafer to make a pump-out port through the first silicon wafer and the layers on the first silicon wafer;

masking and removing material from a first side of a second silicon wafer, to form a recess in the first side of the second silicon wafer;

forming a sealing ring on the first side of the second silicon wafer around the recess; and

positioning the first side of the first silicon wafer next to the first side of the second silicon wafer; and

wherein:

the sealing ring is in contact with at least one of the layers on the first side of the first silicon layer;

the at least one device is within the recess resulting in a chamber containing the at least one device;

the pump-out port is within the sealing ring; and

the first and second silicon wafers are effectively a bonded together set of wafers.

10. The method of claim 9, further comprising:

placing the bonded together set of wafers in an environment of a vacuum wherein a vacuum occurs in the chamber via the pump-out port; and

depositing a layer of material on the second side of the first silicon wafer and the pump-out port on the second side of the first silicon wafer, wherein the chamber is sealed from the environment.

11. The method of claim 10, further comprising baking out the bonded together set of wafers prior to depositing the layer of material on the second side of the first wafer and the pump-out port on the second side of the first silicon wafer.

12. The method of claim 11, wherein the at least one device is a detector.

13. The method of claim 12, further comprising coating the second silicon wafer with antireflection material.

14. The method of claim 11, wherein the second silicon wafer is made from low oxygen silicon or float zone silicon to minimize an absorption peak in an 8–14 micron wavelength region of light going through the second silicon wafer to the at least one device.

15. The method of claim 14, wherein the at least one device is a thermoelectric detector.

16. The method of claim 14, wherein the at least one device is a bolometer.

17. The method of claim 11, wherein the at least one device is an emitter.

18. A method for making a wafer-pair having at least one deposited layer plugged sealed chamber, comprising:

growing a first layer of thermal $SiO_2$ on a first side of a first silicon wafer;

depositing a first layer of $Si_3N_4$ on the first layer of thermal $SiO_2$;

growing a second layer of thermal $SiO_2$ on a second side of the first silicon wafer;

depositing a second layer of $Si_3N_4$ on the second layer of thermal $SiO_2$;

depositing a layer of a first metal on the second layer of $Si_3N_4$;

patterning the layer of the first metal;

depositing a layer of a second metal on the layer of the first metal;

patterning the layer of the second metal;

depositing a third layer of $Si_3N_4$ on the layers of the first and second metals;

etching at least one via through the third layer of $Si_3N_4$, the layers of the second and first metals, the second layer of $Si_3N_4$ and the second layer of thermal $SiO_2$;

etching a pump-out port through the first layer of $SiO_2$ and a first portion of the silicon wafer proximate to the at least one via;

etching within the at least one via through a second portion of the silicon wafer to the pump-out port;

growing a third layer of thermal $SiO_2$ on a first side of a second silicon wafer and a fourth layer of

thermal $SiO_2$ on a second side of the second silicon wafer;

growing a fourth layer of $Si_3N_4$ on the third layer of thermal $SiO_2$ and a fifth layer of $Si_3N_4$ on the fourth layer of $SiO_2$;

patterning and cutting the fourth layer $Si_3N_4$ and the third layer of thermal $SiO_2$ for a bond pad area;

etching a first portion of the second silicon wafer through the fourth $Si_3N_4$ layer and third $SiO_2$ layer for the bond pad area;

patterning and cutting the fifth layer of $Si_3N_4$ and fourth layer of thermal $SiO_2$ for a recess area;

etching a second portion from the second side of the second silicon wafer to form a recess;

applying an optical coating to the second silicon wafer to substantially reduce reflections;

applying a solder ring proximate to a perimeter of the recess, on the second side of the second silicon wafer;

aligning the first silicon wafer with the second silicon wafer, having the first side of the first silicon wafer and the second side of the second silicon wafer face each other;

putting the first and second silicon wafers in a vacuum;

pressing the first and second silicon wafers together with a pressure;

ramping the temperature of the silicon wafers up to a high temperature;

increasing the pressure of the first and second silicon wafers against each other to bond the silicon wafers to each other;

baking out the first and second silicon wafers;

cooling down the first and second silicon wafers under a maintained vacuum;

depositing a layer of a metal on the second side of the second silicon wafer to plug the pump-out port to seal the recess with a vacuum; and

removing the bonded first and second silicon wafers from the vacuum.

**19**. A method for making a wafer-pair having deposited layer plugged sealed chambers, comprising:

growing a thermal layer on a first side of a first silicon wafer;

patterning and removing material from the first silicon wafer and layers on the first side of the first silicon wafer and from a second side of the first silicon wafer to make a plurality of pump-out ports through the first silicon wafer and layers on the first silicon wafer;

masking and removing material from a first side of a second silicon wafer to form a plurality of recesses in the first side of the second silicon wafer;

forming a sealing ring on the first side of the second silicon wafer around each of the plurality of recesses; and

positioning the first side of the first silicon wafer next to the first side of the second silicon wafer; and

wherein:

each sealing ring is in contact with at least one of the layers on the first side of the first silicon layer;

each recess of the plurality of recesses results in a chamber;

each sealing ring encloses at least one pump-out port of the plurality of pump-out ports; and

the first and second silicon wafers are effectively a bonded together set of wafers.

**20**. The method of claim **19**, further comprising:

placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via a pump-out port; and

depositing a layer of material on the second side of the first silicon wafer and the plurality of pump-out out ports on the second side of the first silicon wafer, wherein each chamber is sealed from the environment.

**21**. The method of claim **20**, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer and the plurality of pump-out ports on the second side of the first silicon wafer.

**22**. The method of claim **21**, wherein the set of wafers is cut into a plurality of chips wherein each chip has one or more sealed chambers.

**23**. The method of claim **22**, wherein the one or more sealed chambers contains one or more devices.

**24**. The method of claim **19**, further comprising:

placing the set of wafers in an environment of a gas wherein the gas enters each chamber via a pump-out port; and

depositing a layer of material on the second side of the first silicon wafer and the plurality of pump-out ports on the second side of the first silicon wafer, wherein each chamber is sealed from an ambient environment.

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